AMENDMENT TO THE CLAIMS

1. to 2. (Canceled).

3. (Currently Amended) A memory control device ~~according to claim 2~~, comprising:

a memory controller for controlling an operation of a DRAM and for directly outputting a clock enable signal to said DRAM without any intervening switches;

a power controller for controlling supply of power to said DRAM from a main power supply or a back-up battery power supply and for detecting power stoppage of said main power supply; and

pull-down resistance for pulling down the clock enable signal to low level; and wherein

if said power controller detects the power stoppage of said main power supply during a normal operation, said power controller is configured to switch a power supply for said DRAM from said main power supply to said battery power supply and to instruct a self-refresh mode to said memory controller, so that said memory controller changes the clock enable signal for said DRAM to the low level to establish the self-refresh mode of said DRAM, and

said power controller is further configured to stop the supply of power to said memory controller after said DRAM is set to the self-refresh mode, and, even after the supply of power to said memory controller has been stopped, the clock enable signal is

maintained to the low level by said pull-down resistance, thereby maintaining the self-refresh mode;

wherein, if said power controller detects the power stoppage of said main power supply during the normal operation, said power controller is configured to switch a power supply for said memory controller from said main power supply to said battery power supply, and, after the self-refresh mode of said DRAM is established by said memory controller, to stop the supply of power to said memory controller from said battery power supply; and

wherein the supply of power to said memory controller from said battery power supply is stopped by switching the power supply for said memory controller from said battery power supply to the stopped main power supply.

4. (Original) A memory control device according to claim 3, wherein, when said memory controller informs said power controller of the fact that the self-refresh mode of said DRAM is established, said power controller stops the supplying of power to said memory controller from said battery power supply.

5. to 7. (Canceled)

8. (Currently Amended) A memory control device ~~according to claim 1,~~ comprising:

a memory controller for controlling an operation of a DRAM and for directly outputting a clock enable signal to said DRAM without any intervening switches;

a power controller for controlling supply of power to said DRAM from a main power supply or a back-up battery power supply and for detecting power stoppage of said main power supply; and

pull-down resistance for pulling down the clock enable signal to low level; and wherein

if said power controller detects the power stoppage of said main power supply during a normal operation, said power controller is configured to switch a power supply for said DRAM from said main power supply to said battery power supply and to instruct a self-refresh mode to said memory controller, so that said memory controller changes the clock enable signal for said DRAM to the low level to establish the self-refresh mode of said DRAM, and

said power controller is further configured to stop the supply of power to said memory controller after said DRAM is set to the self-refresh mode, and, even after the supply of power to said memory controller has been stopped, the clock enable signal is maintained to the low level by said pull-down resistance, thereby maintaining the self-refresh mode;

wherein, when said main power supply is normally being ON, after a system reset is cancelled, said memory controller is configured to execute a power-on initial sequence for said DRAM to establish the normal operation, and when said main power supply is restored after the power stoppage, after the system reset is cancelled, an Auto-Refresh Command is issued without executing the power-on initial sequence for said DRAM, thereby entering into the normal operation.

9. (Previously Presented) A memory control device according to claim 8, wherein said power controller makes an instruction signal for the self-refresh mode inactive when said main power supply is normally being ON and maintains the instruction signal to active until immediately after the system reset is cancelled upon restoring of said main power supply after the power stoppage, and

when the system reset is cancelled, said memory controller determines whether or not to execute the power-on initial sequence for said DRAM in accordance with the fact whether the instruction signal is active or not.

10. (Canceled)